UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,683	10/25/2001	Jeffrey M. Calvert	50765	3177

21874 7590 08/31/2004

EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

EXAMINER	
MUTSCHLER, BRIAN L	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 08/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/001,683	CALVERT ET AL.
	Examiner	Art Unit
	Brian L. Mutschler	1753

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004 and 12 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Comments

1. The objection to claims 1 and 12 has been overcome by Applicant's amendment to the claims.

2. The rejection of claims 1, 2, and 14 under 35 U.S.C. 102(b) over Sakamoto et al. has been overcome by Applicant's amendment to the claims requiring the substantial filling of the apertures. While Sakamoto et al. do teach the electroplating of copper within the apertures, it is not clear to what extent the apertures are filled, and therefore the reference does not anticipate the claims.

3. The rejection of claims 8-13 under 35 U.S.C. 103 over EP '078 as the primary reference has been overcome by Applicant's amendment to the claims. Amended claim 8 now requires the step of subjecting the devices to a cathodic activation step plus a seed layer repair process selected from lateral growth enhancement and solution seed layer deposition.

Drawings

4. The drawings were received on July 12, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 7, 14-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 1 005 078 A1, herein referred to as EP '078, in view of either Sakamoto et al. (U.S. Pat. No. 5,788,830) or Carano et al. (U.S. Pat. No. 6,375,731).

Regarding claims 1 and 14, EP '078 discloses a method of electroplating electronic devices, wherein each device has openings with high aspect ratios and a copper-containing seed layer (col. 3, lines 21-31). A cathodic activation step reduces copper oxide on the seed layer (col. 4, lines 37-58). A copper film is electroplated over the seed layer (col. 6, lines 18-35). The cathodic activation step reduces the likelihood of void formation and allows the plating of material within the opening "without having to worry about void formation" (col. 7, lines 19-23).

Regarding claim 2, the seed layer comprises copper and copper oxide (col. 5, line 58 to col. 6, line 5).

Regarding claims 3 and 15, the electronic devices comprise wafers (col. 3, lines 34-38).

Regarding claims 4 and 16, the device further comprises a barrier layer (col. 3, lines 48-52).

Regarding claim 5, the barrier layer may comprise tantalum, titanium, molybdenum, cobalt, nitrides of those materials, or the like (col. 3, lines 48-52).

Regarding claims 7 and 18, the openings have an aspect ratio of at least 2:1 (col. 3, lines 45-47).

The method of EP '078 differs from the instant invention because EP '078 does not disclose a step of testing the electronic device for voids, and if voids are found, using additional seed repair steps, as recited in claims 1 and 14.

EP '078 discloses that the electroplated have a low likelihood of voids (col. 7, lines 19-23). In order to determine if the electroplated layers have a low likelihood of voids, some form of test must be performed to determine the presence or absence of voids. Both Sakamoto et al. and Carano et al. disclose the use of tests to test for voids. Sakamoto et al. teach the use of backlight tests and solder shock tests to test for voids (col. 7, lines 44-51). Carano et al. teach the use of a hot oil thermal shock test to test for voids (col. 7, lines 58-62).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of EP '078 to test the electroplated layer for voids to confirm that the electroplated layers are indeed void-free as taught by Sakamoto et al. and Carano et al. because voids can decrease the reliability of electronic devices and testing for voids determines that the voids are not present.

Since the method of EP '078 does not create voids, seed layer repair steps are not necessary, and the combination meets the minimum process limitations required by the instant claims.

7. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 1 005 078 A1 in view of either Sakamoto et al. (U.S. Pat. No. 5,788,830) or Carano et al. (U.S. Pat. No. 6,375,731), as applied above to claims 1-5, 7, 14-16, and 18, and

further in view of either Reid (U.S. Pat. No. 6,024,857) or Andricacos et al. (U.S. Pat. No. 6,395,164).

EP '078 and Sakamoto et al. or Carano et al. describe a method having the limitations recited in claims 1-5, 7, 14-16, and 18, as explained above in section 6. EP '078 further teaches, "Semiconductor devices continue to be shrunk to smaller dimensions" (col. 1, lines 12-14).

The method described by EP '078 and Sakamoto et al. or Carano et al. differs from the instant invention because they do not disclose that the apertures have a width less than or equal to 1 μm, as recited in claims 6 and 17.

Reid discloses an electroplating method for plating void-free metal layers within apertures having aspect ratios of 4:1 or greater and dimensions less than 0.25 μm (col. 3, lines 4-12; col. 8, lines 12-30).

Andricacos et al. disclose a seed repair method for forming a seed layer that is subsequently electroplated (col. 1, lines 42-51). The method is used for apertures having dimensions less than 0.25 μm and aspect ratios greater than 3:1 (col. 1, lines 28-33).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the method described by EP '078 and Sakamoto et al. or Carano et al. to plate apertures having a width of less than 1 μm as taught by both Reid and Andricacos et al. because smaller apertures lead to faster and smaller electronic devices and Reid and Andricacos et al. teach that such apertures can be similarly electroplated in a void-free manner.

8. Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (U.S. Pat. No. 6,197,181) in view of either Sakamoto et al. (U.S. Pat. No. 5,788,830) or Carano et al. (U.S. Pat. No. 6,375,731).

Regarding claim 8, Chen discloses a method for manufacturing electronic devices comprising the steps of depositing a barrier layer **10** by PVD or CVD and depositing an ultra-thin copper seed layer **15** on the barrier layer by either PVD or CVD (col. 4, lines 1-20). The discontinuous copper seed layer **15** is then enhanced by electroplating copper **18** onto the seed layer (fig. 2C). As seen in Figure 2E, the seed layer enhancement prevents the formation of voids present in the prior art methods as shown in Figure 1. Following the electroplating of copper **18** using an alkaline solution, the device is then subjected to acid electroplating to completely fill the apertures within the substrate (fig. 2D). Chen further teaches that the copper seed layer is typically exposed to an oxygen-containing environment, which results in the formation of copper oxide on the seed layer (col. 7, lines 25-45). Using the alkaline copper bath reduces (i.e., cathodically activates) the copper oxide at the surface of the seed layer (col. 7, lines 25-45).

Regarding claim 9, the electronic devices comprise wafers **30** (col. 5, lines 20-33).

Regarding claims10 and 11, the device comprises a barrier layer **10** made of tantalum nitride or titanium nitride (col. 3, lines 1-10).

Regarding claims 12 and 13, the apertures have a width ≤ 1 μm and an aspect ratio between 1:1 and 1:10 (see fig. 5; scale bar = 1 μm).

The method of Chen differs from the instant invention because Chen does not disclose a step of testing the electronic device for voids, and if voids are found, using additional seed repair steps, as recited in claim 8.

Chen teaches that the enhanced seed layer process avoids the formation of voids present in prior art methods. In order to determine if the electroplated layers have a low likelihood of voids, some form of test must be performed to determine the presence or absence of voids. Both Sakamoto et al. and Carano et al. disclose the use of tests to test for voids. Sakamoto et al. teach the use of backlight tests and solder shock tests to test for voids (col. 7, lines 44-51). Carano et al. teach the use of a hot oil thermal shock test to test for voids (col. 7, lines 58-62).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Chen to test the electroplated layer for voids to confirm that the electroplated layers are indeed void-free as taught by Sakamoto et al. and Carano et al. because voids can decrease the reliability of electronic devices and testing for voids determines that the voids are not present.

Since the method of Chen does not create voids, further seed layer repair steps are not necessary, and the combination meets the minimum process limitations required by the instant claims.

Response to Arguments

9. Applicant's arguments filed on June 4, 2004, have been fully considered but they are not persuasive.

10. Regarding the rejection of claims 1-5, 7-11, 13-16, 18, and 19, Applicant, "Nothing in [EP '078] teaches or suggests how to repair seed layers after voids have been found in apertures that are at least substantially filled with the electrodeposited metal" (see page 8 of Applicant's response). While EP '078 may not teach how to repair seed layers after voids have been found, it is noted that the claimed method does not require the step of finding voids. A method that does not create voids satisfies the limitations recited in the claims.

11. The limitation "wherein a layer of metal electroplated on the seed layer of a first electronic device to at least substantially fill the apertures has voids" does not positively limit the claims. The recited method steps have no relation to the first electronic device. The presence of voids in a first electronic device has nothing to do the performance of the claimed method steps. Prior failures are irrelevant to the performance of the recited method. The instant claims recite a plurality of processes, wherein if a first process does not achieve a void-free deposit, a second process is used. However, the second process is only needed if the first process does not provide void-free deposits. The prior art references cited above (EP '078 and Chen) teach the formation of void-free deposits on the first attempt. In order to ascertain whether or not the deposits are free of voids, it would be obvious to test the deposits for voids. Once the void-free nature of the deposits is ascertained, no modifications to the procedure are necessary.

12. Applicant further argues that Sakamoto fails to teach or suggest apertures that are at least substantially filled with metal (see page 8 of Applicant's response). This argument is not persuasive because Sakamoto is not relied upon to teach substantially filling apertures. EP '078 and Chen both teach methods wherein the apertures are substantially filled. Sakamoto is relied upon to teach methods for testing electroplated features for voids.

13. Regarding the rejection of claims 6, 12, and 17, Applicant argues that Reid does not teach the formation of a seed layer (see page 9 of Applicant's response). The teachings of Reid are not relied upon to teach the formation of a seed layer. Reid teaches a method for electroplating vias having a prescribed aspect ratio. Similarly, Applicant argues that Andricacos et al. do not teach the repair of seed layers. Likewise, the teachings of Andricacos et al. are not relied upon to teach the repair of seed layers. Such repair techniques are already taught by the primary references of EP '078 and Chen.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (571) 272-1341. The examiner can normally be reached on Monday-Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BLM
August 23, 2004

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700